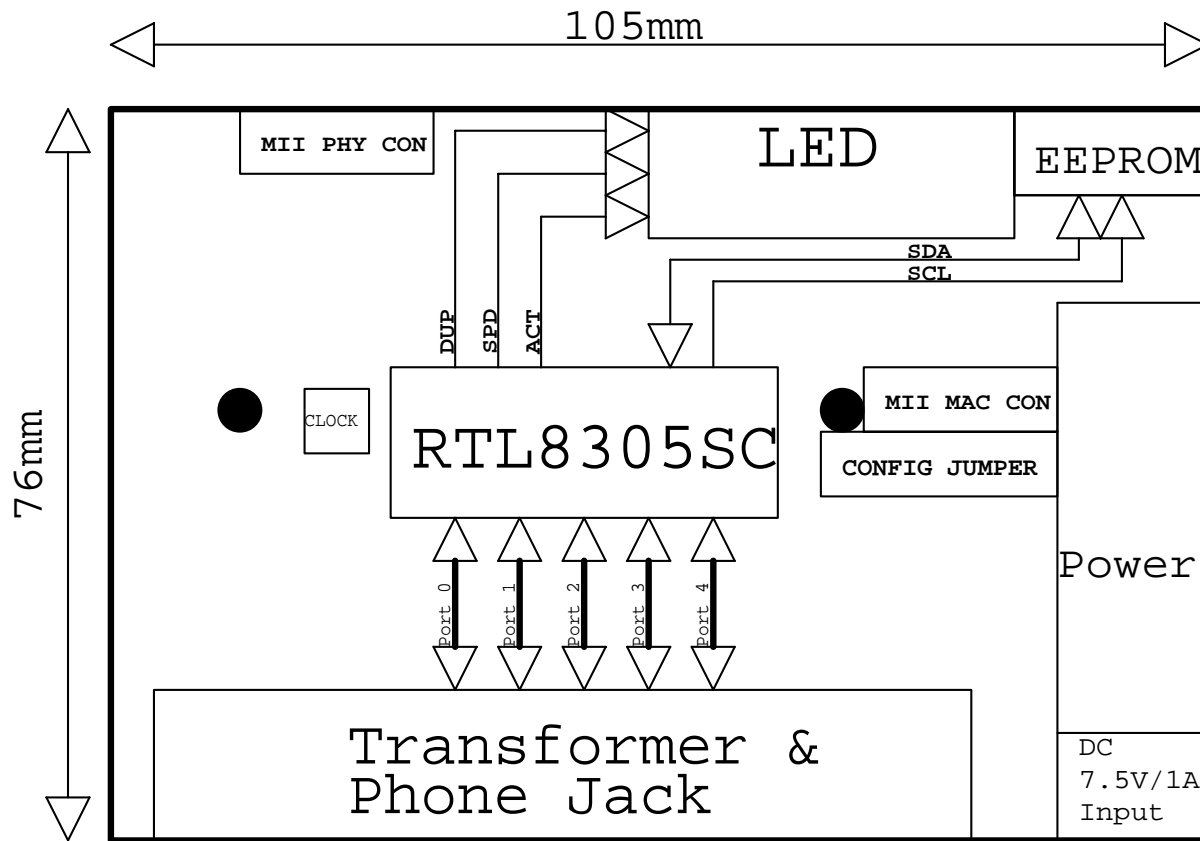


RTL8305SC Demo Board 5 port UTP



Note:

- 1: The demo board is 2 layer PCB and 1 side SMD for RTL8305SC.
 - 2: Crystal shunt capacitor C50 and C51 should use 18pF.
 - 3: L5~L8 are used for EMI test, optional for customers.
 - 4: R13, IBREF resister should use 1.96K ohm.
 - 5: J2 is for Port4 PHY circuit MII interface connector.
 - 6: J3 is for Port4 MAC circuit MII interface connector.
 - 7: R75 and R76 is for internal test, don't need for customers.
 - 8: R78 is used for PHY2TXEN pull down resister.
- When L2 dump switch test should not be assembled.
- When enable Dual MII function, the resister should be assembled.

RTL8305SC Demo Board Revision History

1.0	First release
1.1	Add R77 for MRXDV_PTXEN and R78 for PHY2TXEN pull down resisters when enable Port 4 MII function and Dual MII function.
2.0	PCB layout change to v.2.0 Power solution: C45 change to 470pF & R53, R54, R56, L11 short and removed for improve EMI. L5, L6, L7, L8 change to 1000pF/2KV for improve EMI. Seperate RV1, RV2 circuit, and add RV4, RV5. RV1-RV5 change to 68pF/2KV for improve EMI. Add C55, C56, C57 at DC Jack CN1 for improve EMI. J1 change to 1*4 connector and add 3.3V at pin 4. J4 change to 2*7 connector and remove EN_DEFER setting pin. J3.3 MDC & J3.4 MCIO pin change to NC pin.

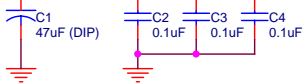
RTL8305SC 5 Port Switch Demo Board Configuration Resister

R8	Defer enable/disable, open to enable and short to disable
T3/3, 4	Port 4 Link Status Control, short with jumper to force Port 4 link
R9	Port 4 Duplex Control, open for full duplex and short for half duplex
T3/5, 6	Port 4 Speed Control, open for 100Mbps and short for 10Mbps
R10	Port 4 Flow Control, open for enable and short for disable full duplex flow control
T3/7, 8	Port 4 Mode Control, [11]: UTP/MII MAC; [10]: 100Base-FX; [01]: MII PHY; [00]: SNI PHY
T3/9, 10	Disable Dual MII, short to enable Dual MII function
R11	Broadcast storm control enable/disable, open to disable and short to enable
R12	Backpressure enable/disable, open to enable and short to disable
T3/11, 12	Broadcast Input/Output drop, RH1/RH2 for input drop and RL1/RL2 for output drop
T3/13, 14	
R13, R14	
T3/15, 16	
R15	
R6	
R7	
RH1/RH2, RL1/RL2	

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Title		Author: Alex Lin
RTL8305SC DEMO BOARD		
Size A	Document Number BLOCK DIAGRAM	Rev 2.0
Date: Thursday, August 05, 2004	Sheet 1 of 4	

DVDD33 DVDD33



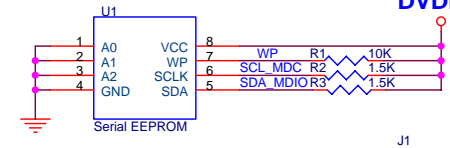
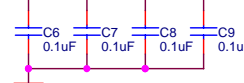
(4) DUP3_GYMODE
(4) SPD3_DISARP
(4) ACT3_EN48P1
(4) DUP4_SETGP
(4) SPD4_DISVLAN
(4) ACT4_DISFCOFF

DUP3_GYMODE
SPD3_DISARP
ACT3_EN48P1
DUP4_SETGP
SPD4_DISVLAN
ACT4_DISFCOFF

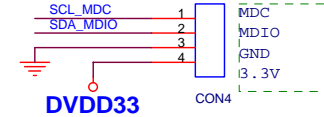
DVDD18



DVDD18

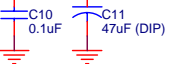


DVDD33



DVDD33

AVDD33



(4) ACT2_P4ANEG
(4) SPD2_GXANEG
(4) DUP2_GYANEG

(4) ACT1_GYSPD
(4) SPD1_GXFULL
(4) DUP1_GYFULL

(4) ACT0_BCINDROP
(4) SPD0_MAX1536
(4) DUPO_AGBACK

(4) 8305SC_X1
(4) 8305SC_X2

(4) VCTRL
DTEST2
DTEST1

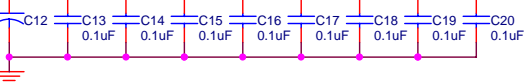
(3) RD0+ RXIN0
(3) RD0+ RXIP0
(3) TD0+ TXON0
(3) TD0+ TXON1
(3) TD1+ TXON1
(3) TD1+ TXON2
(3) TD1+ TXON3
(3) RD1+ RXIN1
(3) RD1+ RXIN2
(3) RD2+ RXIP2
(3) RD2+ RXIP3
(3) TD2+ TXON2
(3) TD2+ TXON3
(3) TD3+ TXON3
(3) TD3+ RXIP3
(3) RD3+ RXIN3
(3) RD4+ RXIN4
(3) RD4+ RXIP4
(3) TD4+ TXON4

(3) RD0+ RXIN0
(3) RD0+ RXIP0
(3) TD0+ TXON0
(3) TD0+ TXON1
(3) TD1+ TXON1
(3) TD1+ TXON2
(3) TD1+ TXON3
(3) RD1+ RXIN1
(3) RD1+ RXIN2
(3) RD2+ RXIP2
(3) RD2+ RXIP3
(3) TD2+ TXON2
(3) TD2+ TXON3
(3) TD3+ TXON3
(3) TD3+ RXIP3
(3) RD3+ RXIN3
(3) RD4+ RXIN4
(3) RD4+ RXIP4
(3) TD4+ TXON4

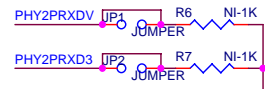
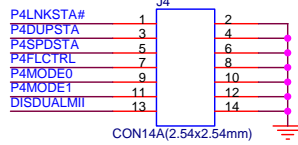
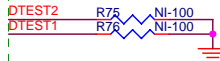
(3) RD0+ RXIN0
(3) RD0+ RXIP0
(3) TD0+ TXON0
(3) TD0+ TXON1
(3) TD1+ TXON1
(3) TD1+ TXON2
(3) TD1+ TXON3
(3) RD1+ RXIN1
(3) RD1+ RXIN2
(3) RD2+ RXIP2
(3) RD2+ RXIP3
(3) TD2+ TXON2
(3) TD2+ TXON3
(3) TD3+ TXON3
(3) TD3+ RXIP3
(3) RD3+ RXIN3
(3) RD4+ RXIN4
(3) RD4+ RXIP4
(3) TD4+ TXON4

(3) RD0+ RXIN0
(3) RD0+ RXIP0
(3) TD0+ TXON0
(3) TD0+ TXON1
(3) TD1+ TXON1
(3) TD1+ TXON2
(3) TD1+ TXON3
(3) RD1+ RXIN1
(3) RD1+ RXIN2
(3) RD2+ RXIP2
(3) RD2+ RXIP3
(3) TD2+ TXON2
(3) TD2+ TXON3
(3) TD3+ TXON3
(3) TD3+ RXIP3
(3) RD3+ RXIN3
(3) RD4+ RXIN4
(3) RD4+ RXIP4
(3) TD4+ TXON4

AVDD18



Note: Lay on solder
only for test,
don't need for customer



Mark on board
DIS_BCSTM

EN_BKPRS

EN_DEFER

P4_LNK_STA#

P4_DUP_STA

P4_SPD_STA

P4_FCTRL_STA

P4MODE[0]

P4MODE[1]

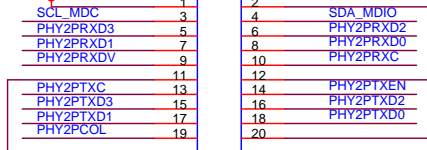
DISDUALMII

RTL8305SC

Layout Note:

1.96K(1%) Close to 8305SC

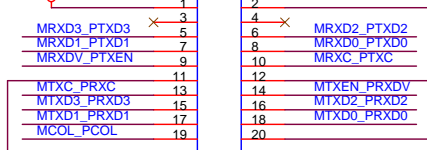
DVDD33



Mark on board

Port4 PHY
Circuit MII

DVDD33



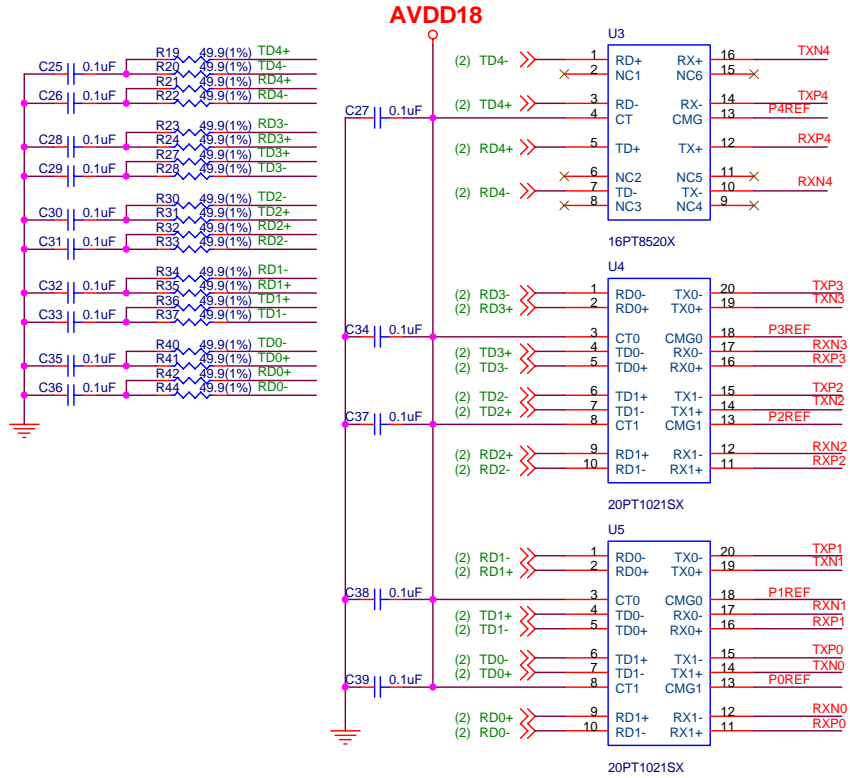
Mark on board

Port4 MAC
Circuit MII

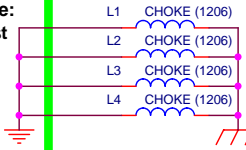
Realtek Semiconductor Corp.

Title		RTL8305SC DEMO BOARD		Author: Alex Lin	
Size	B	Document Number	RTL8305SC	Rev	2.0
Date:	Thursday, August 05, 2004	Sheet	2	of	4

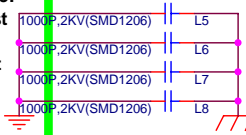
ANALOG POWER



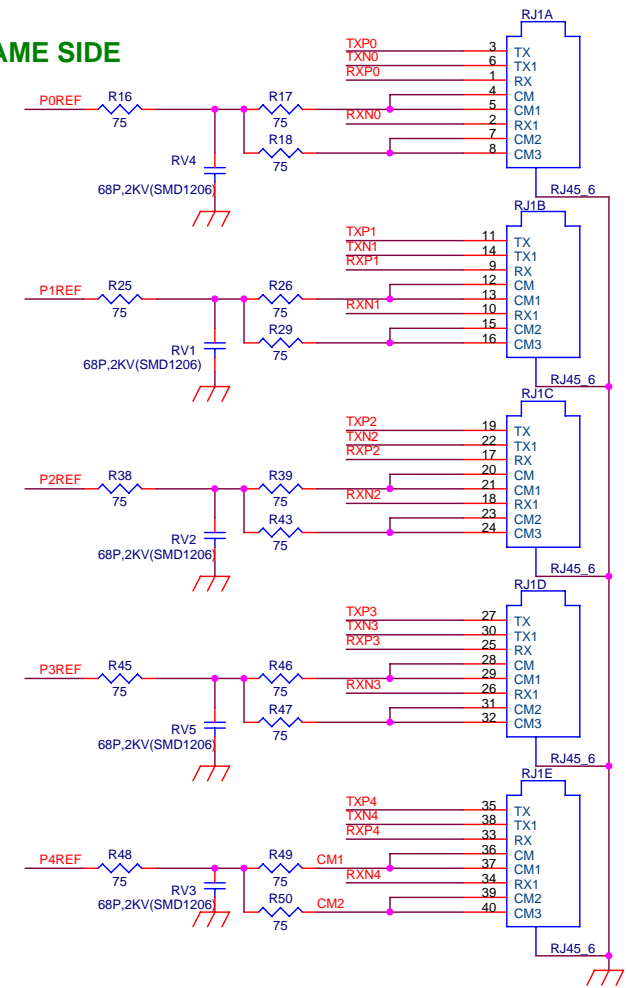
Layout Note
For EMI test
Lay on
solder



Layout Note
For EMI test
Lay on
component



FRAME SIDE



Realtek Semiconductor Corp.

Title	RTL8305SC DEMO BOARD
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Author: Alex Lin

Size	Document Number
B	PhoneJack & XFORMER

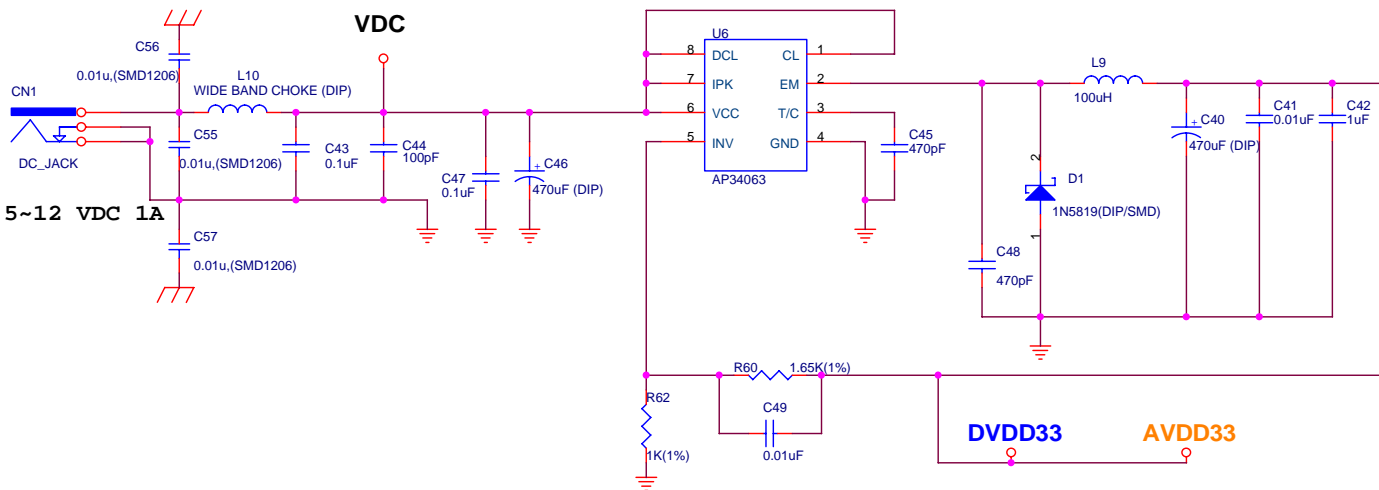
Rev	2.0
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Date: Thursday, August 05, 2004

Sheet 3 of 4

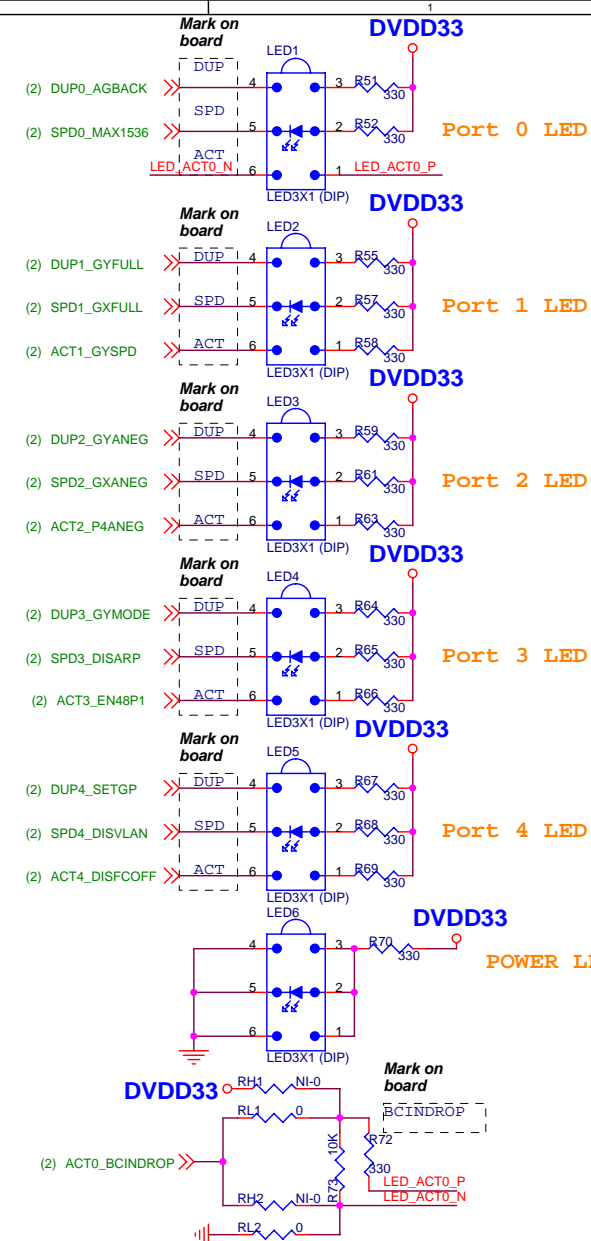
POWER 3.3V

VDC



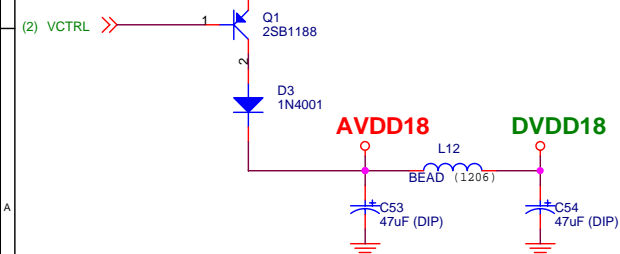
$$V_{out} = 1.25 * (R60 + R62) / R62$$

LED



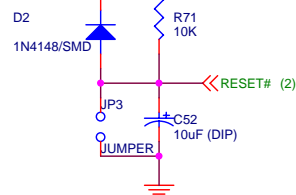
POWER 1.8V

AVDD33



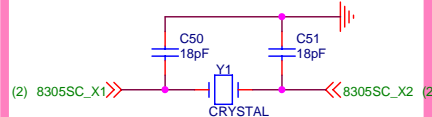
RESET

DVDD33



CLOCK

Layout Note:
Close to RTL8305SC



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Title		RTL8305SC DEMO BOARD		Author: Alex Lin	
Size	B	Document Number	POWER & CLOCK & RESET & LED		Rev
					2.0
Date:	Thursday, August 05, 2004		Sheet	4	of 4